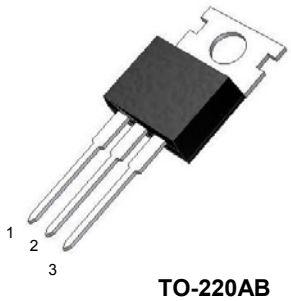
TAK CHEONG®

Preliminary Data Sheet

TFP2N65

N-Channel Power MOSFET

1.9A, 650V, 7.5Ω



1 = Gate
2 = Drain
3 = Source

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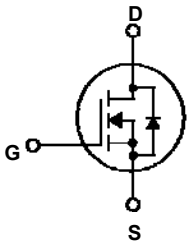


General Description

The N-Channel MOSFET is used an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance. This device is well suited for high efficiency switched mode power suppliers, active power factor correction, electronic lamp ballasts based half bridge topology.

Features

- Robust high voltage termination
- Avalanche energy specified
- Diode is characterized for use in bridge circuits
- Source to Drain diode recovery time comparable to a discrete fast recovery diode.

DEVICE MARKING DESIGNATION:
Line 1 = TC Brand
Line 2 = Device Type

ABSOLUTE MAXIMUM RATINGS (T_C =25°C, unless otherwise noted)

Symbol	Parameter		Value	Units
V_{DSS}	Drain- Source Voltage		650	V
V_{GSS}	Gate-Source Voltage		±30	V
I_D	Drain Current		1.9	A
I_{DM}	Drain Current Pulsed		7.6	A
P_D	Power Dissipation	(Note 2)	55	W
	Derating factor above 25℃		0.44	W/℃
E_{AS}	Single Pulsed Avalanche Energy	(Note 1)	127	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 2)	5.5	mJ
T_J	Operating Junction Temperature		150	℃
T_{stg}	Storage Temperature Range		- 55 to +150	℃

Notes:
1. L=65mH, I_{AS}=1.9A, V_{DD}=50V, R_G=25Ω, Starting T_J=25℃
2. Repetitive Rating: Pulse width limited by maximum junction temperature.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.26	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	℃/W

ELECTRICAL CHARACTERISTICS

Off Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Sounce Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30V, V_{DS} = 0V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30V, V_{DS} = 0V	--	--	-100	nA

On Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = 250uA	2.0	--	4.0	V
$R_{DS(ON)}$	On-Resistance	V_{GS} = 10V, I_D = 0.9A	--	5.0	7.5	Ω

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ciss	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	--	200	260	pF
Coss	Output Capacitance		--	30	40	pF
Crss	Reverse Transfer Capacitance		--	9	12	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 325V, I_D = 1.9A, R_G = 50 Ω (Note 3 & 4)	--	12	34	nS
tr	Turn-On Rise Time		--	14	38	nS
$t_{d(off)}$	Turn-Off Delay Time		--	36	82	nS
tr	Turn-Off Fall Time		--	18	46	nS
Qg	Total Gate Charge	V_{DS} = 520V, I_D = 1.9A, V_{GS} = 10V (Note 3 & 4)	--	8	11	nC
Qgs	Gate-Source Charge		--	1.5	--	nC
Qgd	Gate-Drain Charge		--	4.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min.	Typ,	Max.	Unit
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	8.0	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 1.9A	--	--	1.5	V
Trr	Reverse Recovery Time	V_{GS} = 0V, I_S = 1.9A, dI_F / dt = 100A/uS (Note 3)	--	241	--	nS
Qrr	Reverse Recovery Charge		--	0.95	--	uC

Notes:

3. Pulse Test: Pulse width < 300us, Duty cycle ≤ 2%.
4. Basically not affected by working temperature.

TYPICAL CHARACTERISTICS

Fig 1. On-State Characteristics

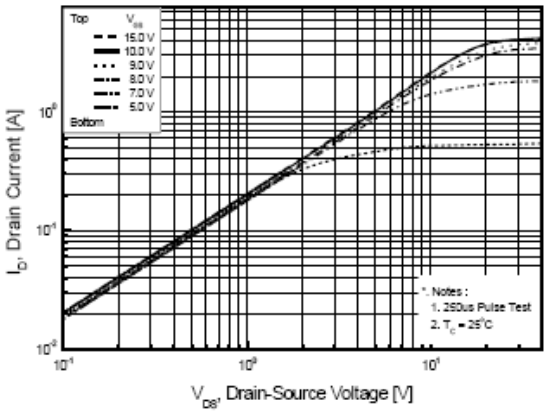


Fig 2. Transfer Characteristics

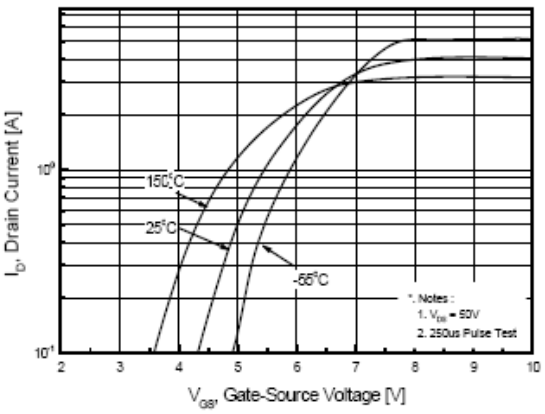


Fig 3. On Resistance Variation vs.
Drain Current and Gate Voltage

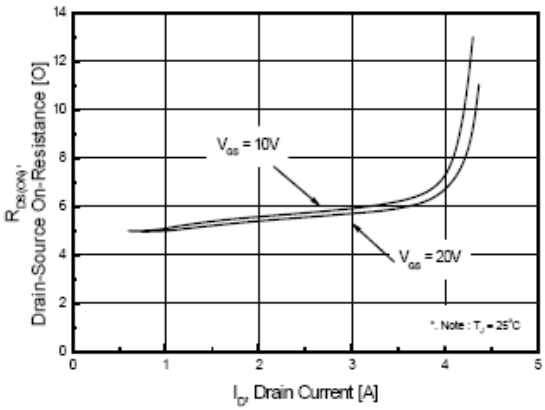


Fig 4. On State Current vs.
Allowable Case Temperature

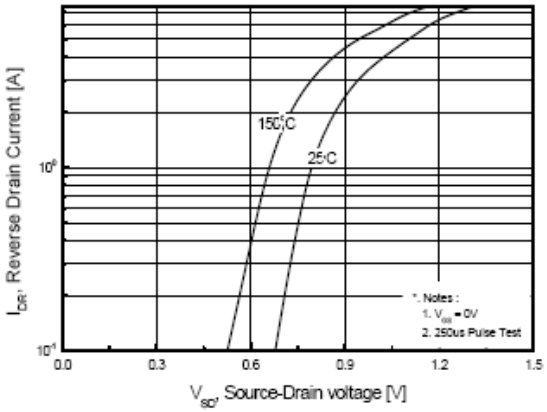


Fig 5. Capacitance Characteristics
(Non-Repetitive)

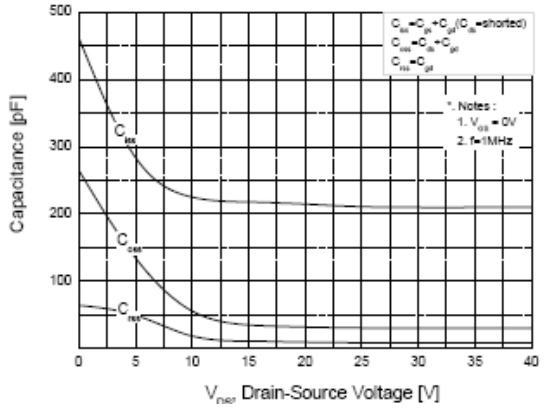


Fig 6. Gate Charge Characteristics

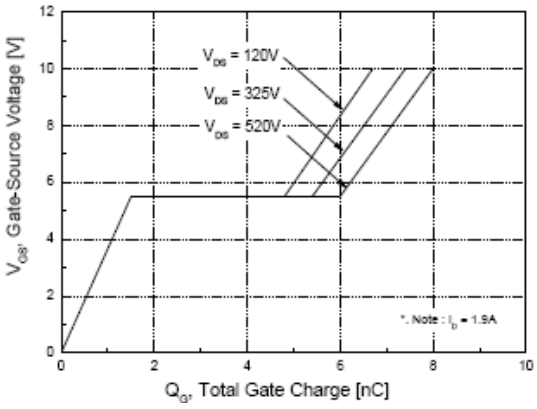


Fig 7. Breakdown Voltage Variation vs. Junction Temperature

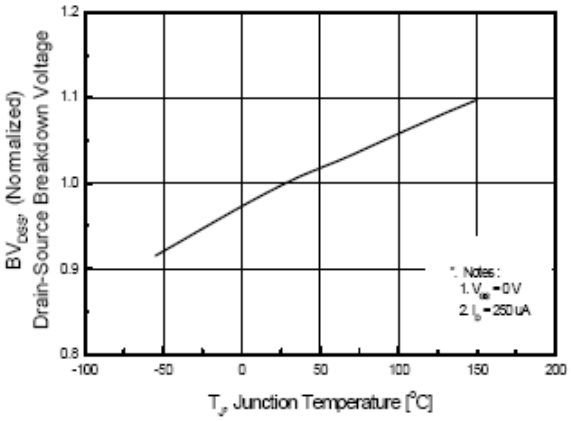


Fig 8. On-Resistance Variation vs. Junction Temperature

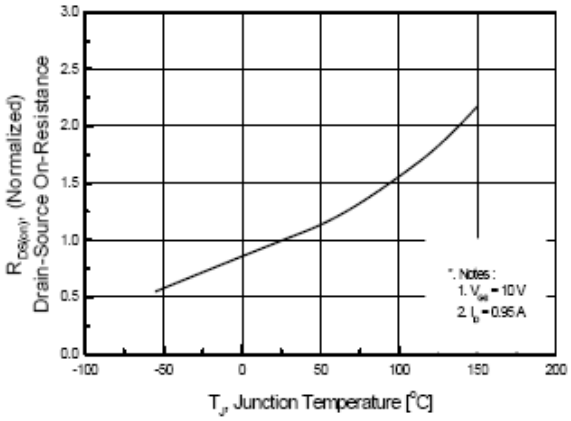


Fig 9. Maximum Safe Operating Area

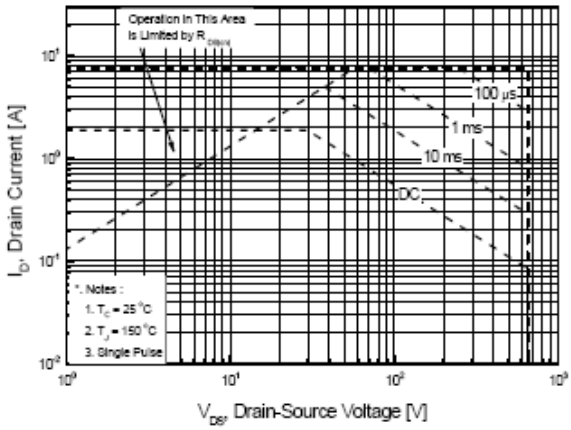


Fig 10. Maximum Drain Current vs. Case Temperature

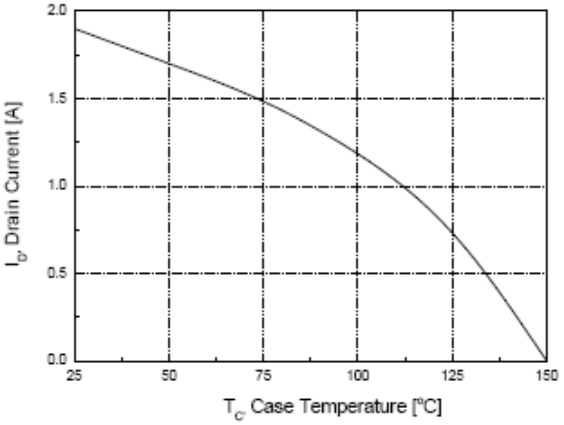


Fig 11. Transient Thermal Response Curve

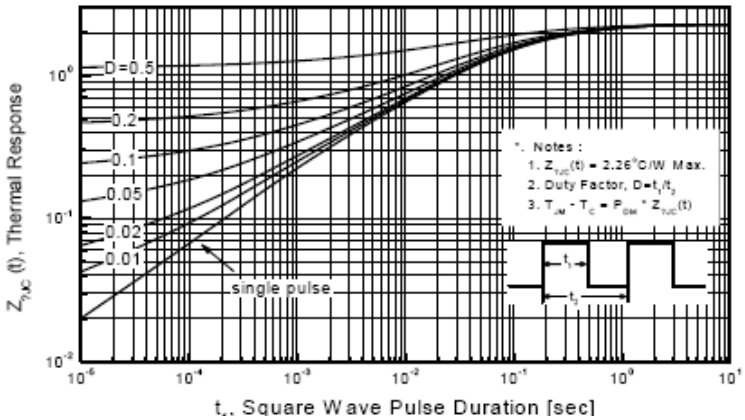


Fig. 12. Gate Charge Test Circuit & Waveforms

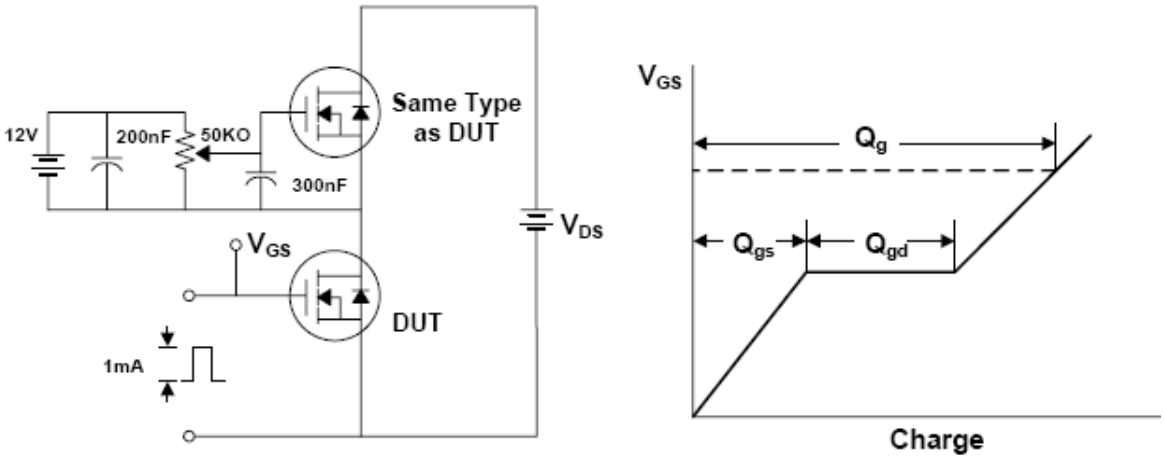


Fig 13. Switching Time Test Circuit & Waveforms

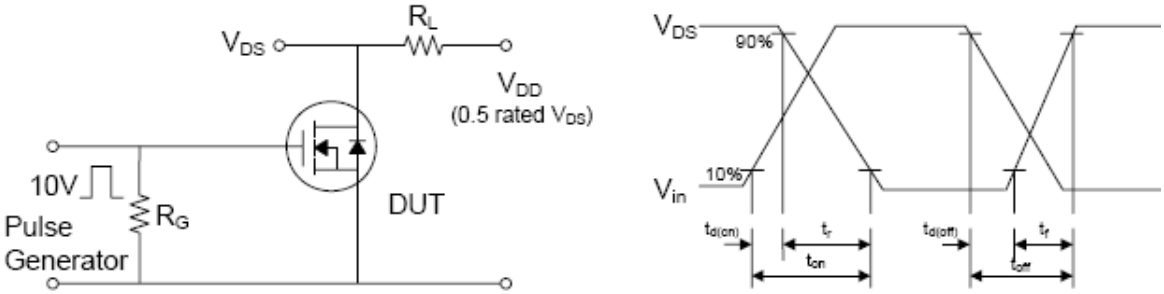


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

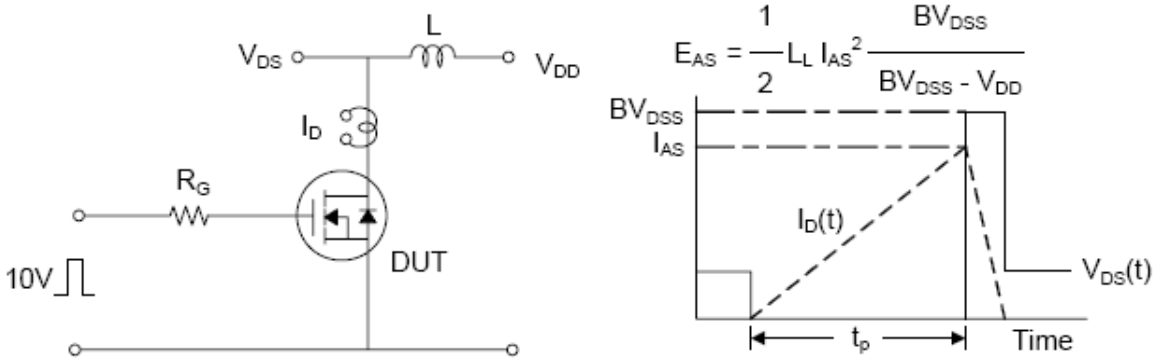
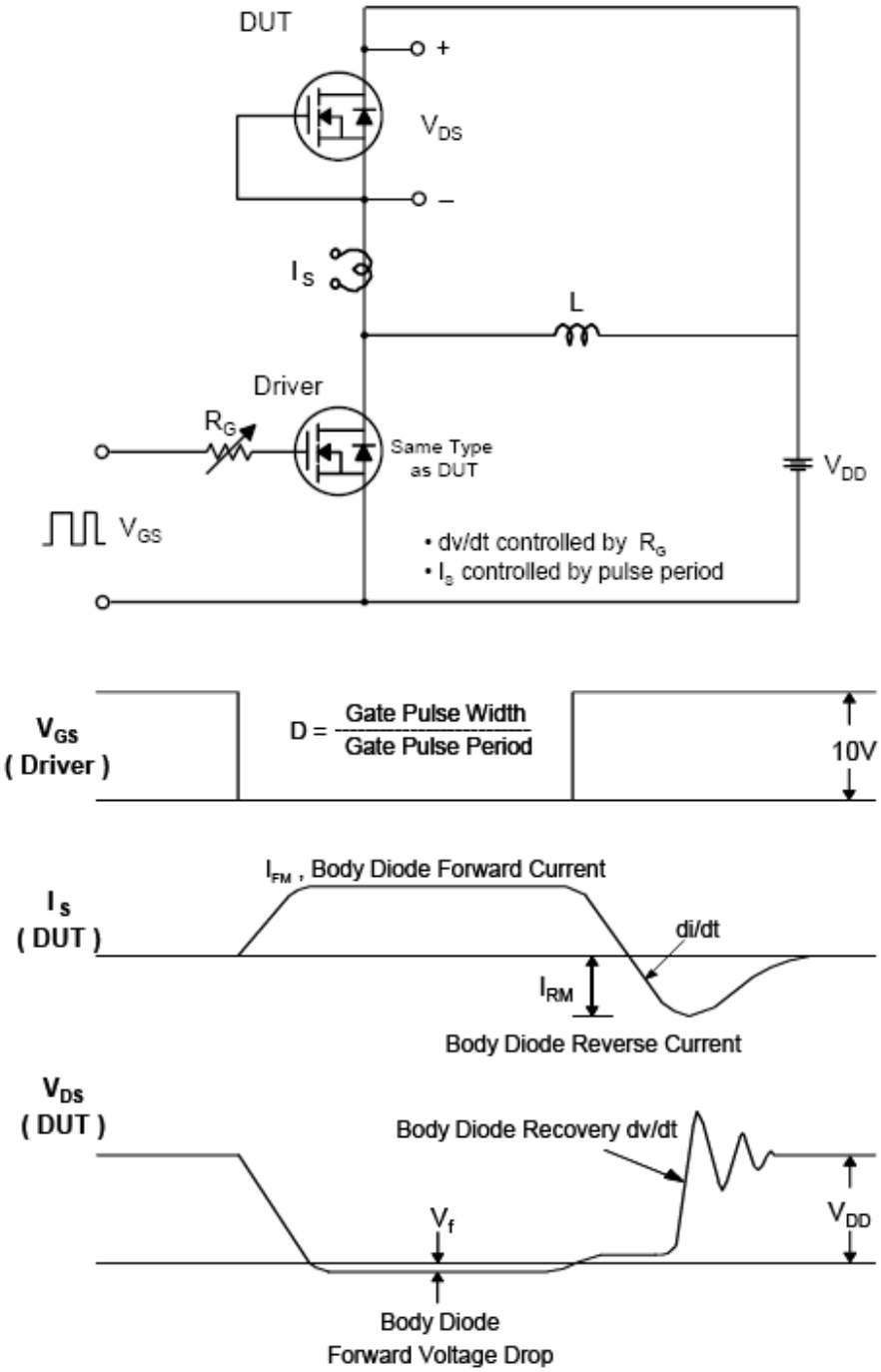
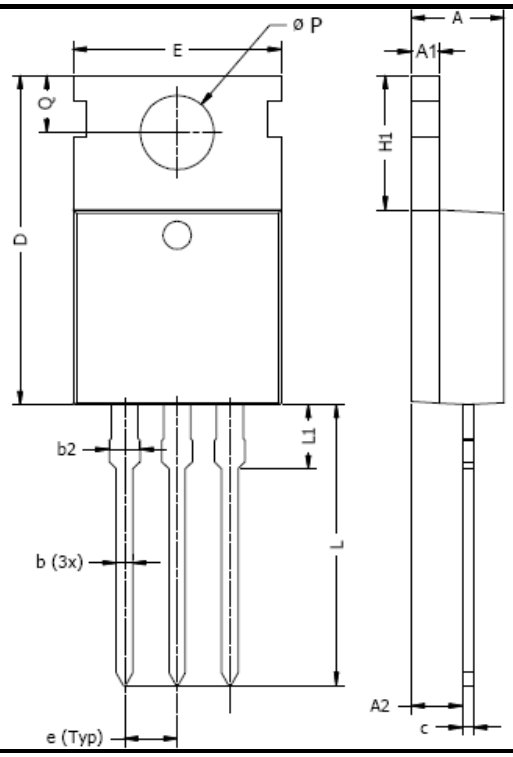


Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO220AB PACKAGE OUTLINE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.6	4.8	0.142	0.189
A1	1.2	1.4	0.047	0.055
A2	2.0	2.9	0.079	0.114
b	0.4	1.0	0.016	0.039
b2	1.2	1.8	0.047	0.071
c	0.36	0.6	0.014	0.024
D	14.2	16.5	0.559	0.650
e	2.34	2.74	0.092	0.108
E	9.7	10.6	0.382	0.417
H1	5.8	6.85	0.228	0.270
L	12.7	14.7	0.500	0.579
L1	2.7	3.3	0.106	0.130
ØP	3.5	4.0	0.138	0.157
Q	2.54	3.4	0.100	0.134

NOTE: Above package outline conforms to JEDEC TO-220AB

NOTICE

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